Fig. 1

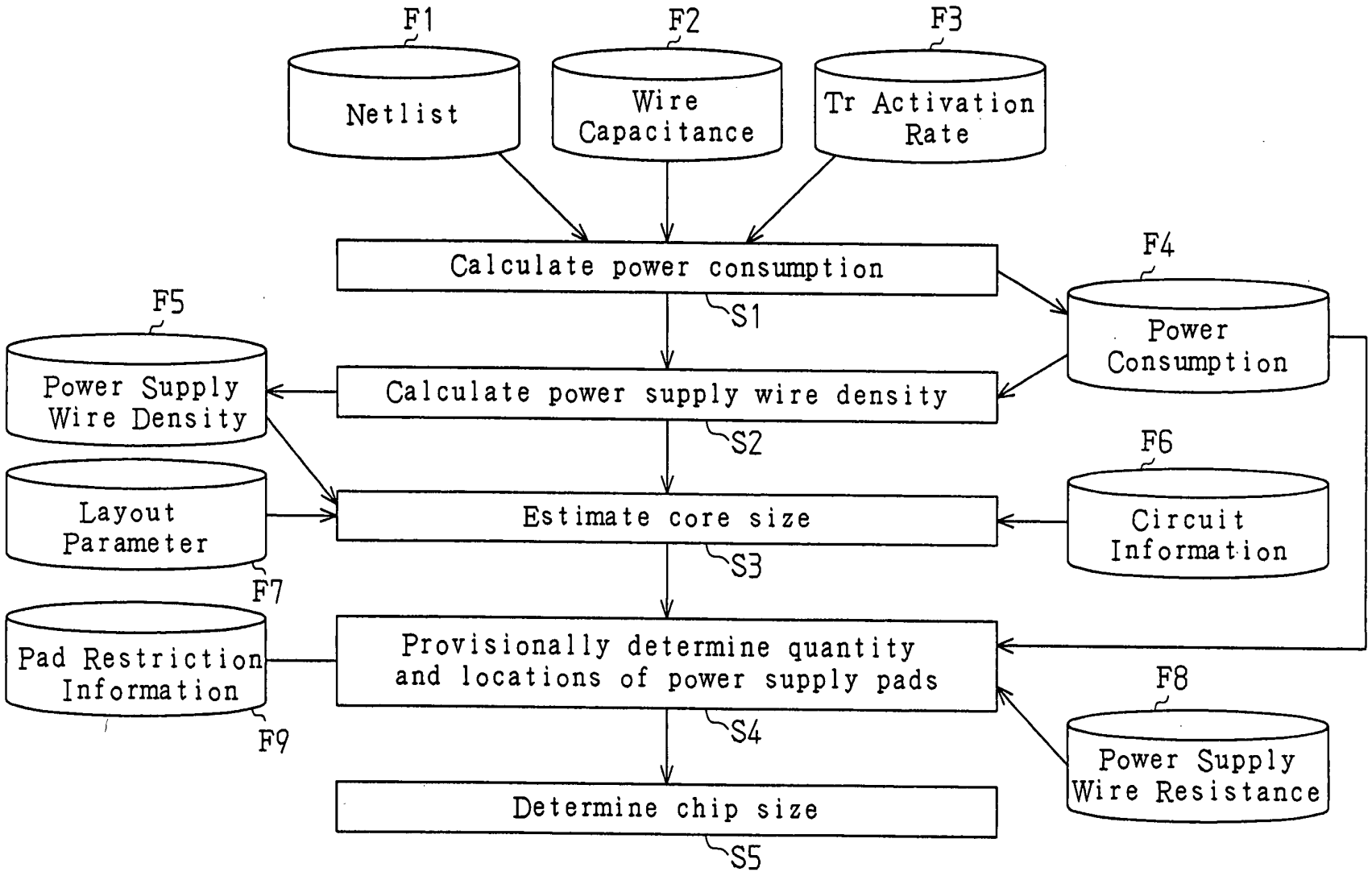

F1
Netlist
F2
Wire Capacitance
F3
Tr Activation Rate
Calculate power consumption
S1
F4
Power Consumption
F5
Power Supply Wire Density
Calculate power supply wire density
S2
F6
Layout Parameter
F7
Estimate core size
S3
Circuit Information
Pad Restriction Information
F9
Provisionally determine quantity and locations of power supply pads
S4
F8
Power Supply Wire Resistance
Determine chip size
S5

Fig. 2

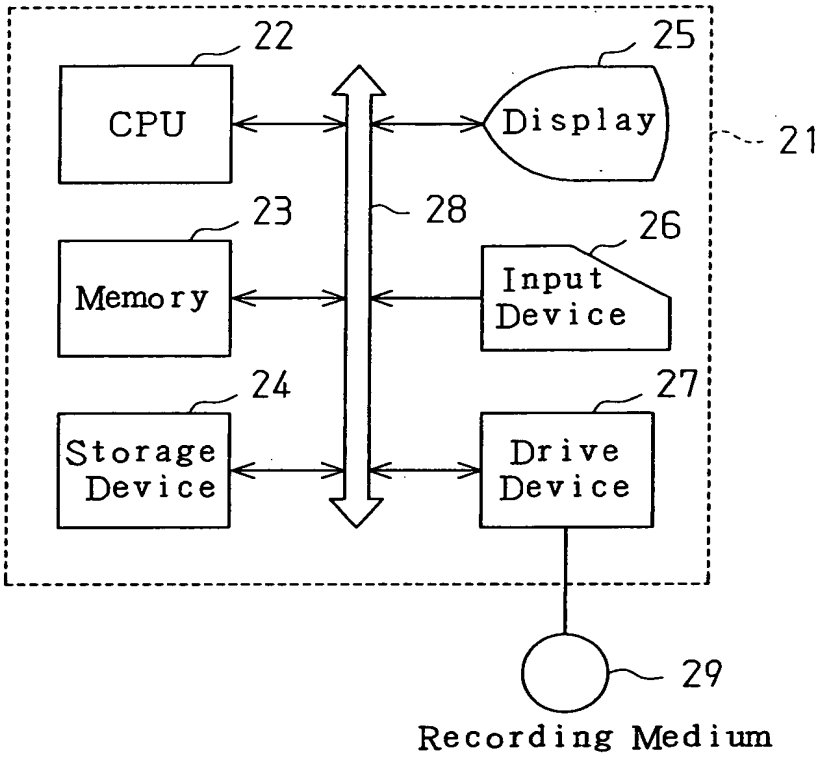

22
CPU
25
Display
21
23
28
26
Memory
Input Device
24
27
Storage Device
Drive Device
29
Recording Medium

Fig. 3

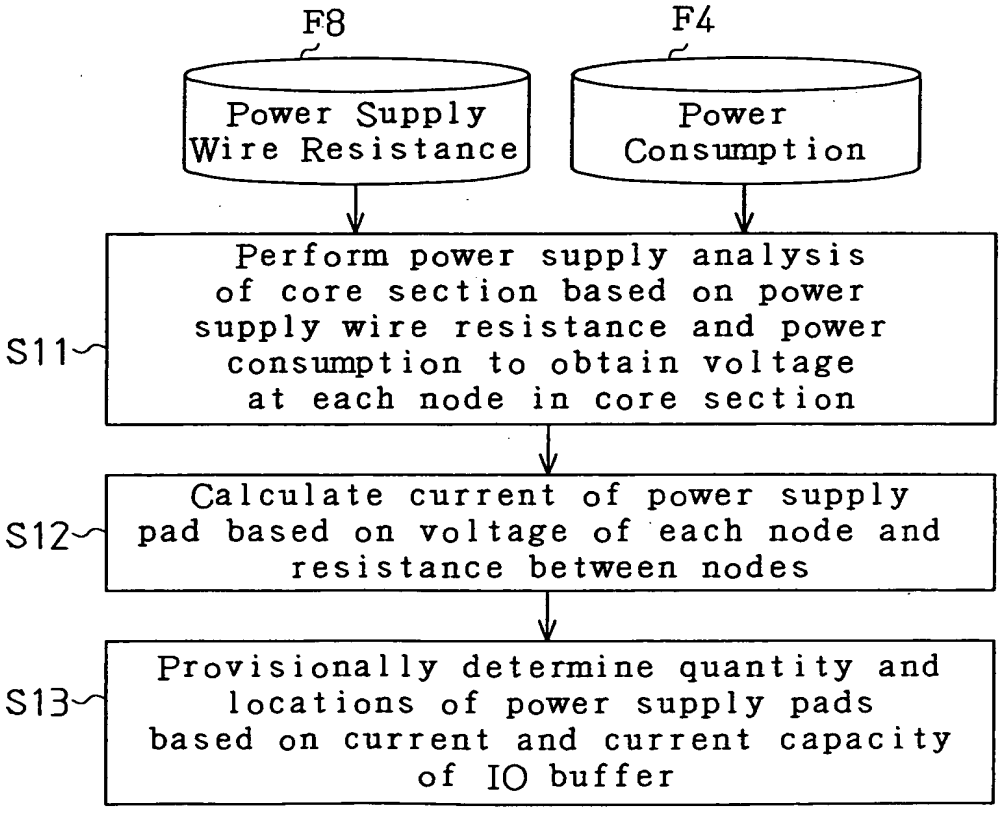

F8
F4
Power Supply Wire Resistance
Power Consumption
S11
Perform power supply analysis of core section based on power supply wire resistance and power consumption to obtain voltage at each node in core section
S12
Calculate current of power supply pad based on voltage of each node and resistance between nodes
S13
Provisionally determine quantity and locations of power supply pads based on current and current capacity of IO buffer

Fig. 4

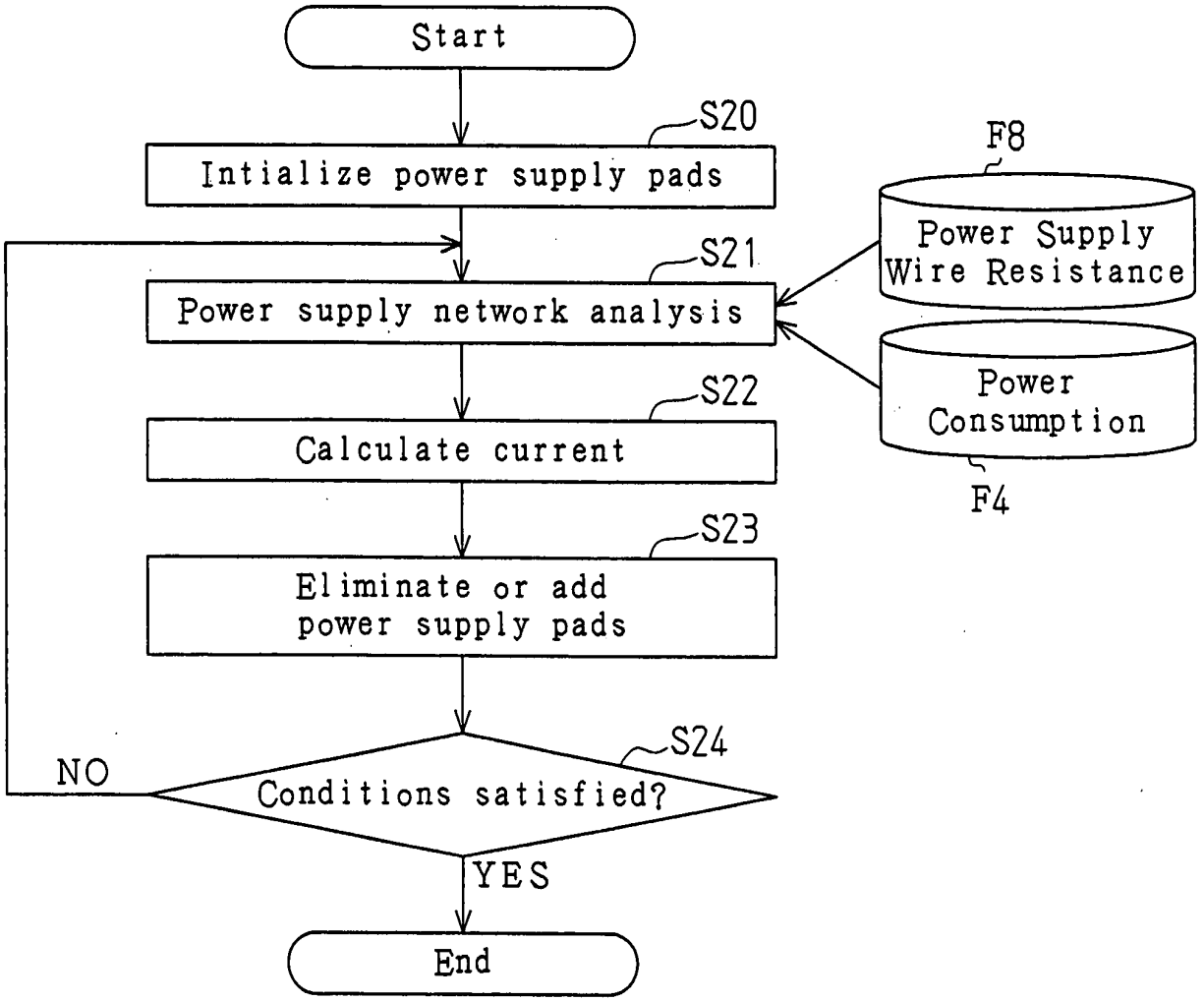

Start
S20
Intialize power supply pads
S21
Power supply network analysis
S22
Calculate current
S23
Eliminate or add power supply pads
S24
Conditions satisfied?
NO
YES
End
F8
Power Supply Wire Resistance
Power Consumption
F4

Fig. 5A

(Initial state)

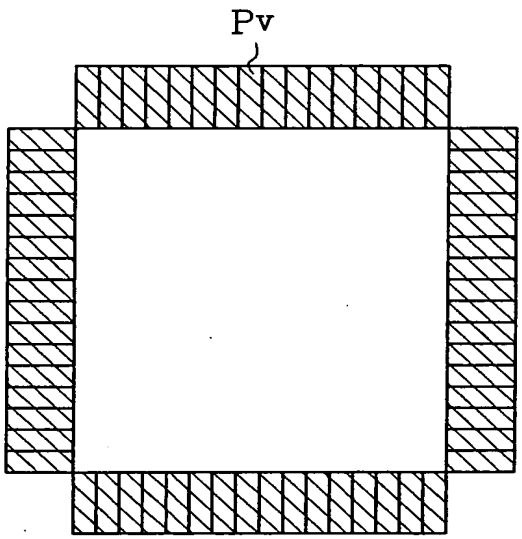


Fig. 5B

(Eliminated state)

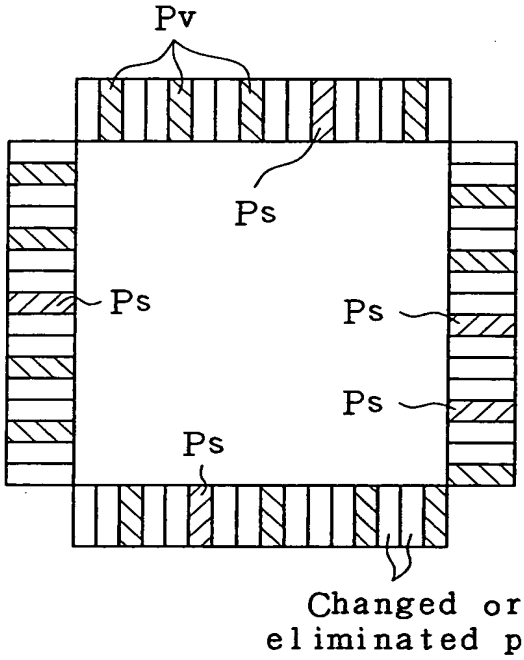


Fig. 6

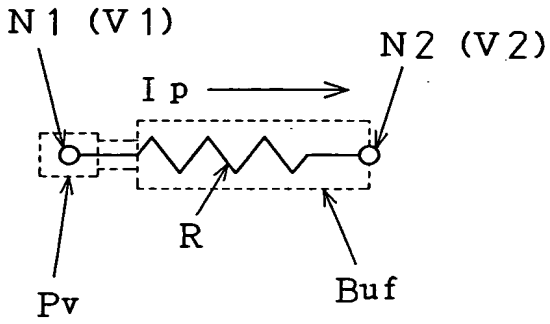


Fig. 7

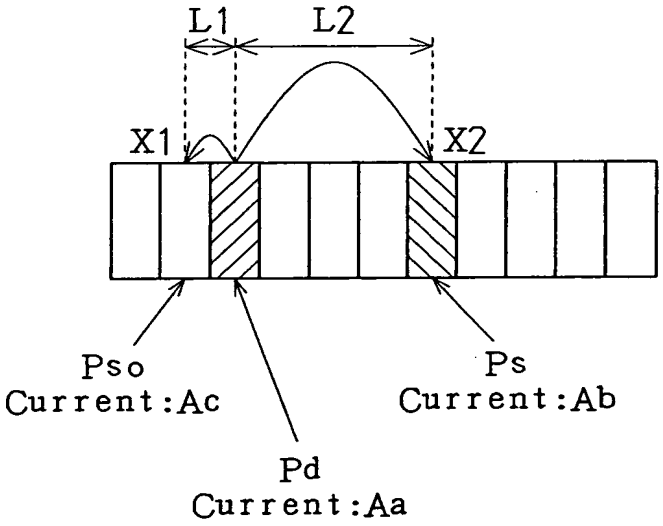

L1
L2
X1
X2
Pso
Current:Ac
Ps
Current:Ab
Pd
Current:Aa

Fig. 8

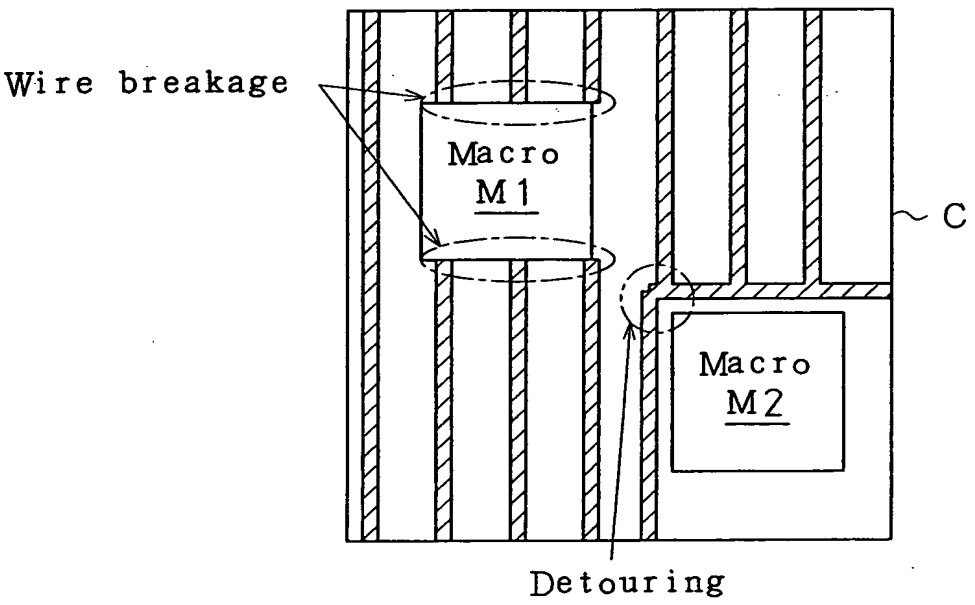

Wire breakage
Macro
M1
C
Macro
M2
Detouring

Fig. 9

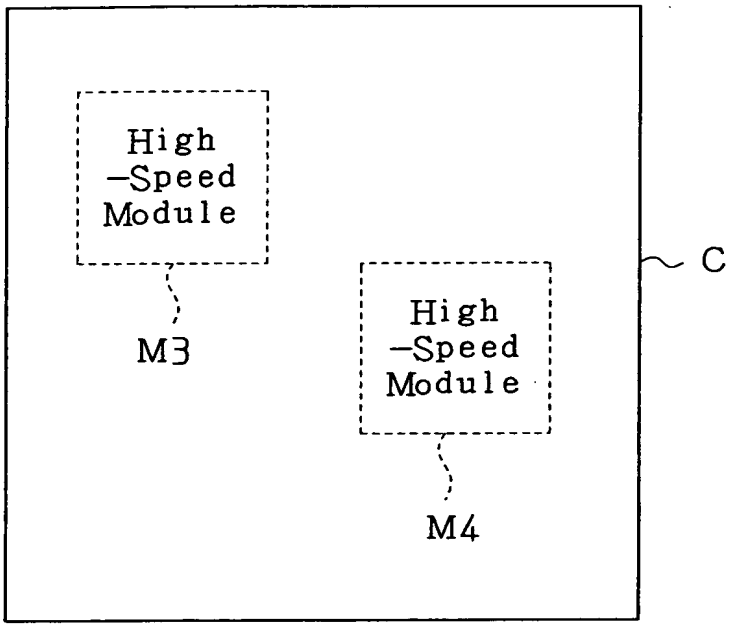

High
-Speed
Module
M3
High
-Speed
Module
M4
C

Fig. 10

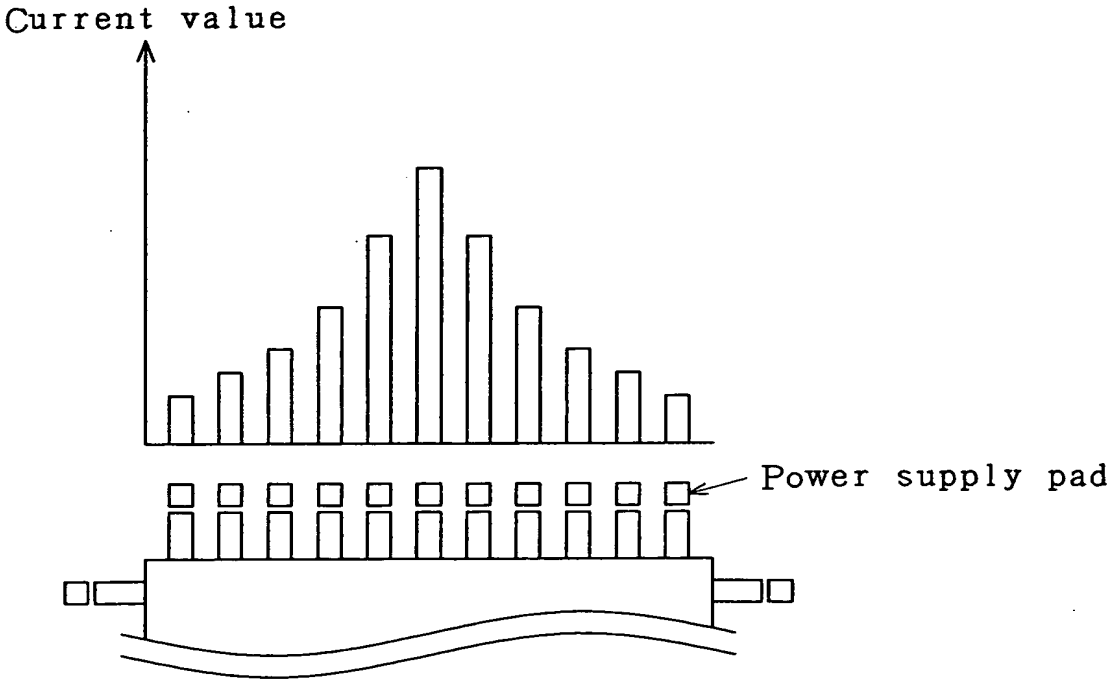

Current value
Power supply pad

Fig. 11

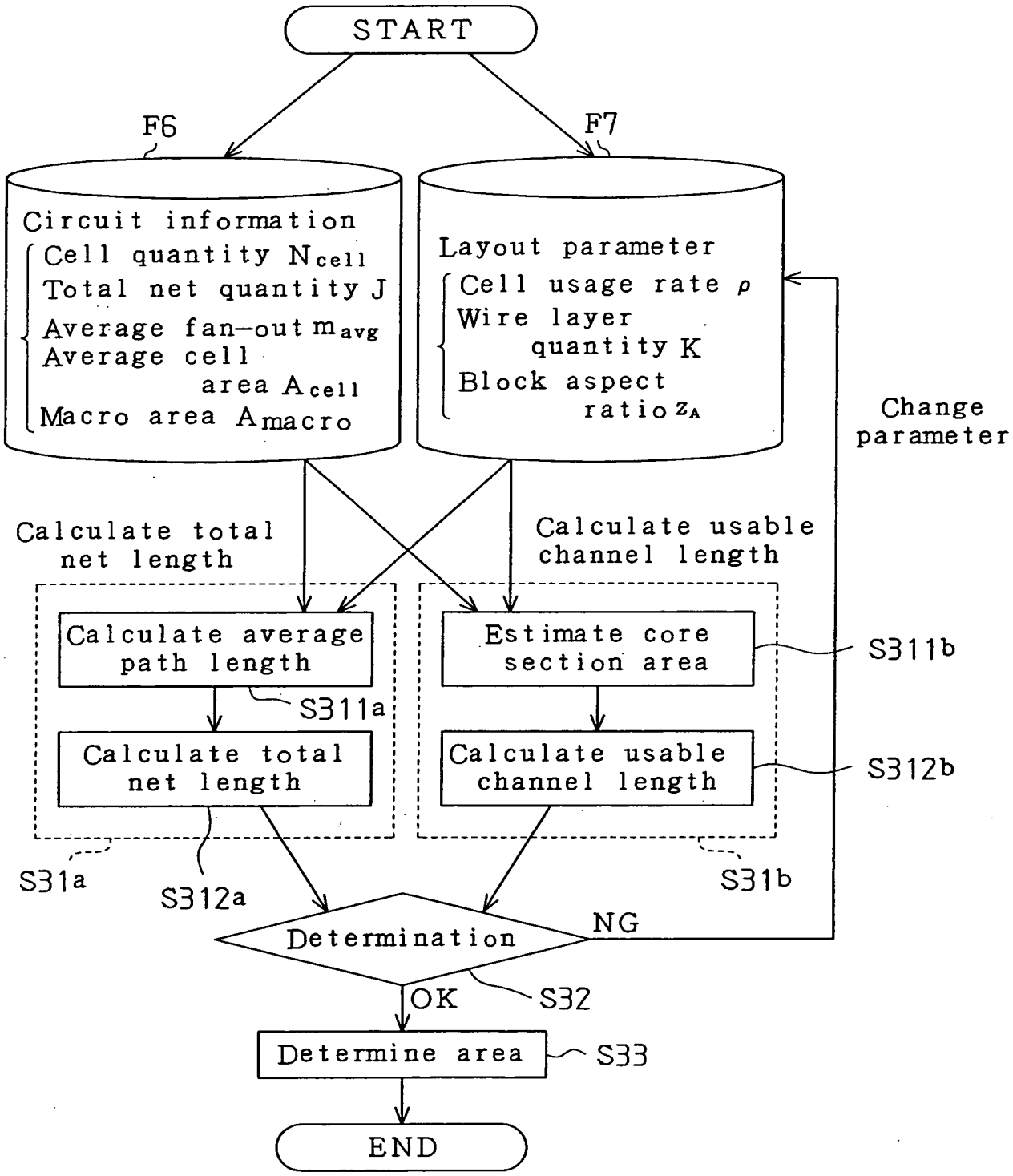

START
F6
F7
Circuit information
Cell quantity N_{cell}
Total net quantity J
Average fan-out m_{avg}
Average cell area A_{cell}
Macro area A_{macro}
Layout parameter
Cell usage rate ρ
Wire layer quantity K
Block aspect ratio z_A
Change parameter
Calculate total net length
Calculate usable channel length
Calculate average path length
S311a
Calculate total net length
Estimate core section area
S311b
Calculate usable channel length
S312b
S31a
S312a
S31b
Determination
NG
OK
S32
Determine area
S33
END

Fig. 12

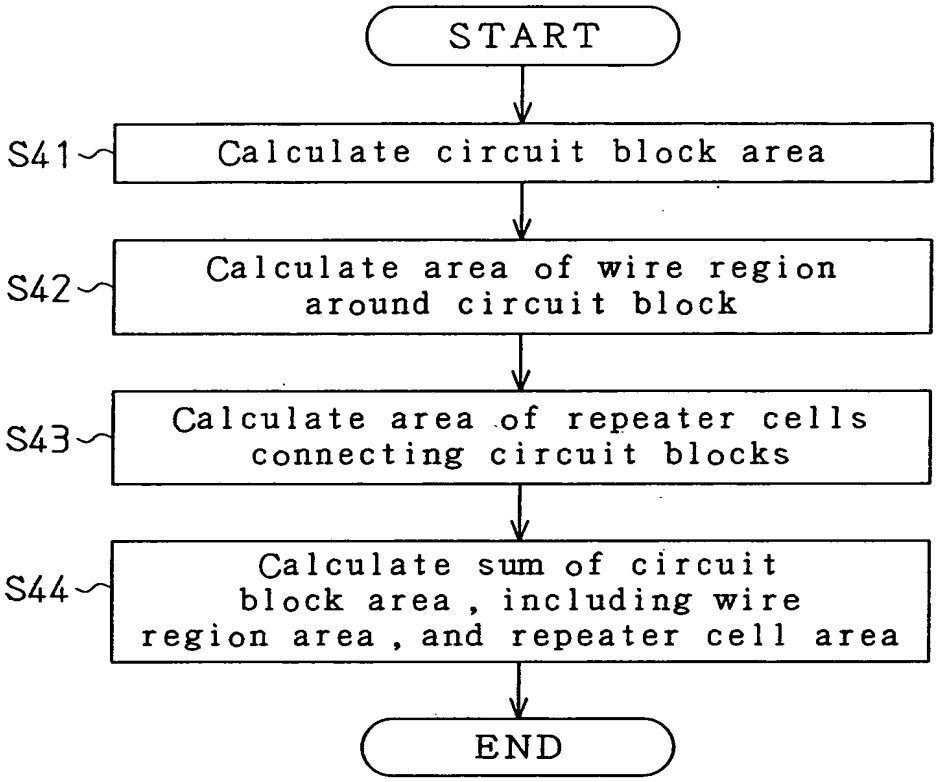

START
S41
Calculate circuit block area
S42
Calculate area of wire region around circuit block
S43
Calculate area of repeater cells connecting circuit blocks
S44
Calculate sum of circuit block area , including wire region area , and repeater cell area
END

Fig. 13

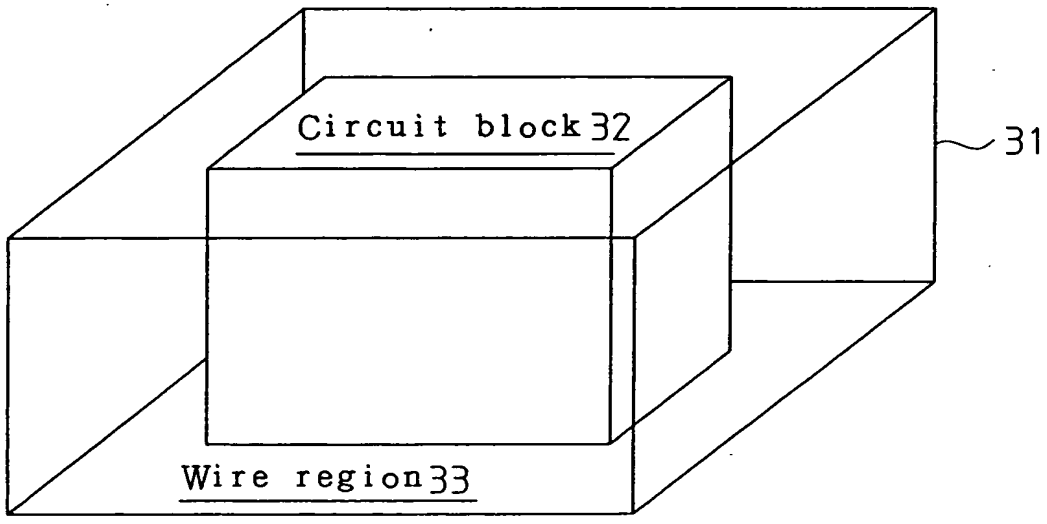

Circuit block 32
31
Wire region 33

Fig. 14

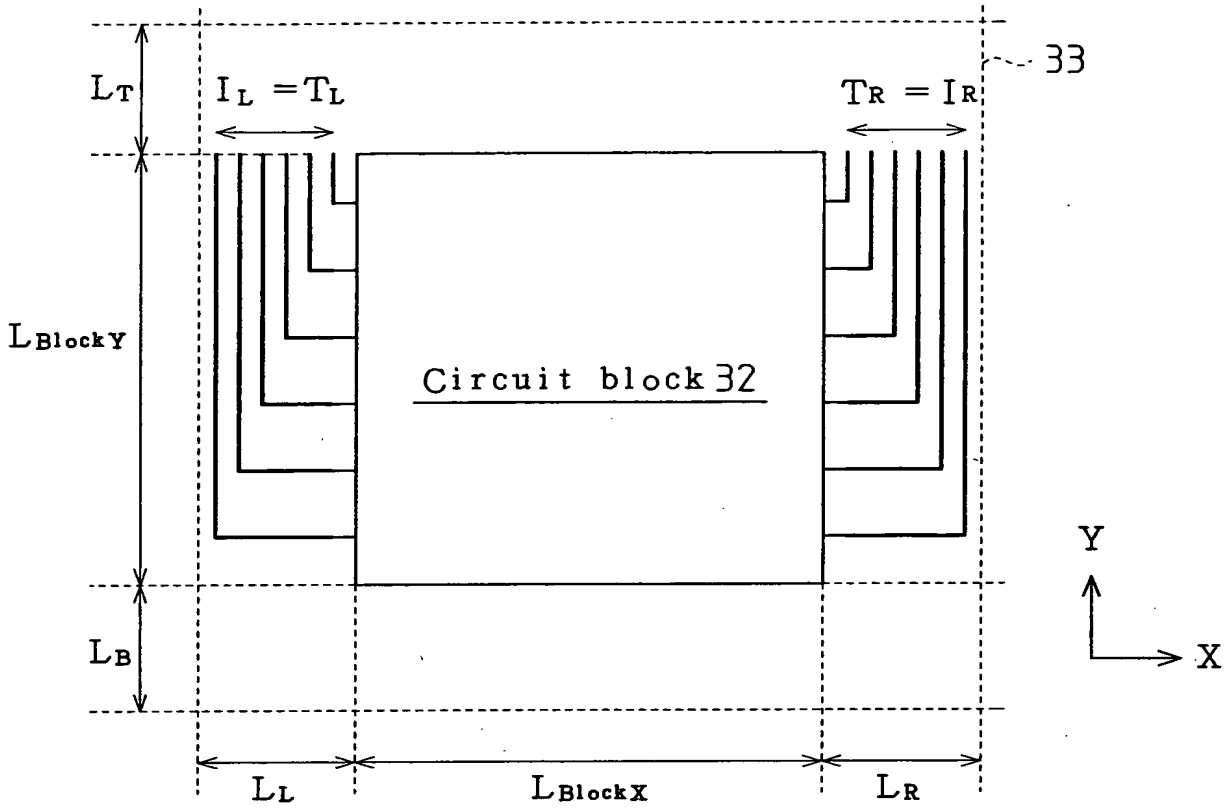

33
L_T
$I_L = T_L$
$T_R = I_R$
L_{BlockY}
Circuit block 32
L_B
Y
X
L_L
L_{BlockX}
L_R

Fig. 15

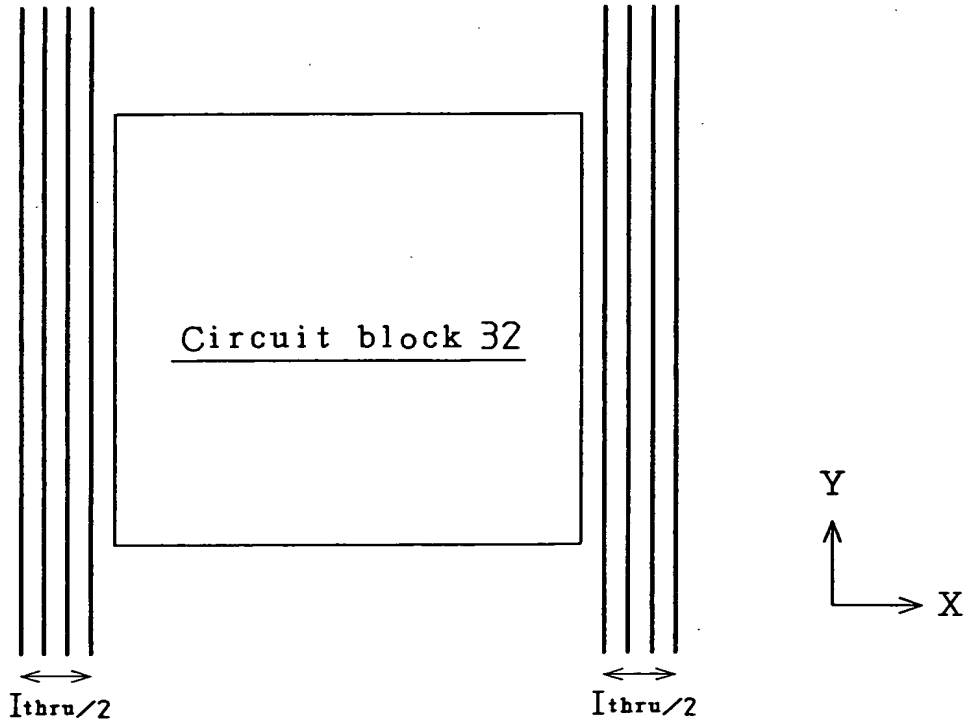
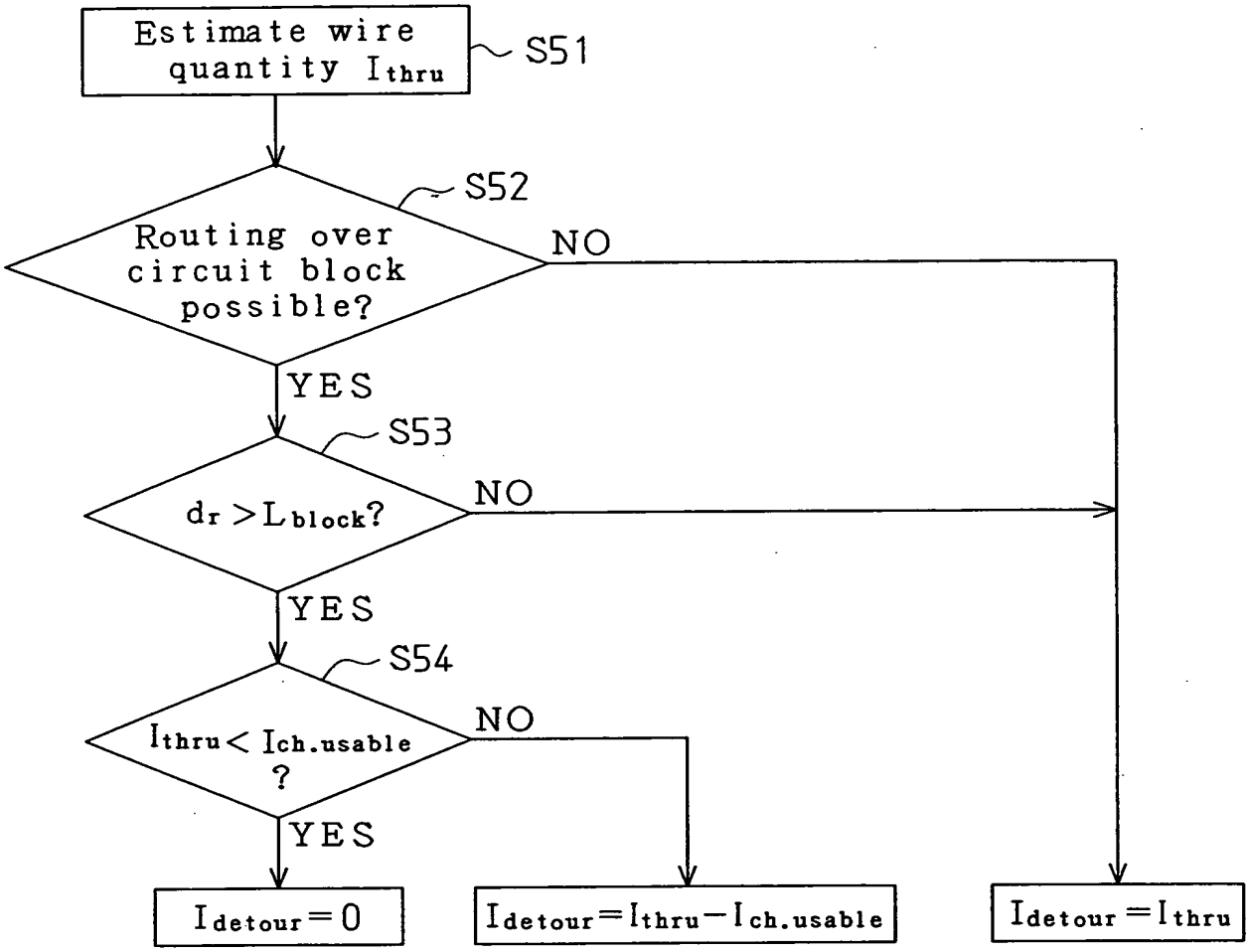

Circuit block 32
Y
X
$I_{thru}/2$
$I_{thru}/2$

Fig. 16


Estimate wire quantity I_{thru}
S51
S52
Routing over circuit block possible?
NO
YES
S53
$d_r > L_{block}$?
NO
YES
S54
$I_{thru} < I_{ch.usable}$?
NO
YES
$I_{detour} = 0$
$I_{detour} = I_{thru} - I_{ch.usable}$
$I_{detour} = I_{thru}$